A SERIES-CONNECTED MULTILEVEL INVERTER TOPOLOGY FOR MEDIUM-VOLTAGE BLDC MOTOR DRIVE APPLICATIONS

CH. BRAHMAIAH[1], CH. SRINIVAS RAO[2], M. BABA FAKRUDDIN[3]

[1]M-tech Student Scholar, Department of Electrical & Electronics Engineering, C.V.S.R College of Engineering, Hyderabad; Andhra Pradesh, India

[2]Assistant Professor, Department of Electrical & Electronics Engineering, C.V.S.R College of Engineering, Hyderabad, Andhra Pradesh, India

[3]M-tech Student Scholar, Department of Electrical & Electronics Engineering, C.V.S.R College of Engineering, Hyderabad, Andhra Pradesh, India.

ABSTRACT

Present day drive types are the Induction motor drives with voltage source inverters. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required "fundamental" sinusoidal components, but also pulses of voltage i.e. "ripple" voltage. Moreover the voltage waveforms produced by the inverter has sharp edges. The rate of change of voltage with respect to time i.e. dv/dt is very high at these edges, of the order of 500–5000 V/µs. The two-level inverter topology has attracted attention in low power low voltage drive applications where as Three Level inverter topology has attracted attention in high power High performances voltage drive applications. The Main purpose of these three level inverter topologies is to provide a three phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms the benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. In this paper, a topology with series connection of three-phase three-level inverters is proposed, which addresses the problems of medium-voltage drives. The simulation results based on Matlab/Simulink are discussed in detail in this paper.

KEYWORDS: Dynamic Voltage Restorer, d-q-o Controller, Voltage Swells, Distribution System, Sensitive Load

INTRODUCTION

Power electronic inverters are widely used in various industrial drive applications. To overcome the problems of the limited voltage and current ratings of power semiconductors devices, some kinds of series and/or parallel connections are necessary. Recently, the multilevel inverters have received more attention in literature due to their ability to synthesize waveforms with a better harmonic spectrum and to attain higher voltages. They are applied in many industrial applications such as ac power supplies, static Var compensators, and drive

System, etc. Multilevel inverters have very important development for high power medium voltage AC drives. Quite a lot of topologies have found industrial approval; Neutral Point Clamped, flying capacitor, H-bridge, cascaded with separated DC source, several control and modulation strategies have been developed Pulse Width Modulation (PWM), Sinusoidal PWM, Space Vector PWM and Selective harmonic eliminations etc. One of the significant advantages of multilevel configuration is the harmonics reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2, 3]. These multilevel inverters, in case of *m*-level, can increase the capacity by

(*m*-1) times than that of two-level inverter through the series connection of power semiconductor devices without additional circuit to have uniform voltage sharing. Comparing with two level inverter system having the same capacity, multilevel inverters have the advantages that the harmonic components of line-to-line voltages fed to load, switching frequency of the devices and EMI problem could be decreased [1]. The output voltage waveform of a multilevel inverter is composed of a number of levels of voltages starting form three levels and reaching infinity depending upon the number of the dc sources. The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltage sources. These dc voltages may or may not be equal to one another. These dc sources can be obtained from batteries, fuel cells, or solar cells.

Conventionally, each phase of a cascaded multilevel converter requires '*n*' dc sources for 2*n* + 1 levels in applications that involve real power transfer. These dc sources are assumed to have identical amplitudes. Similar voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters or by cascading a number of two-level inverters. However, the multilevel NPC inverters suffer from dc-bus imbalance, device underutilization problems and unequal ratings of the clamped diodes, etc., which are not very serious problems for inverters with three levels or lower. The capacitor voltage imbalance for a five-level one is presented in which suggest the need of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The cascaded H-bridge topology suffers from the drawbacks of the usage of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

POWER-CONVERTER TOPOLOGY

The proposed general configuration of "*n*" number of three level inverters connected in series is shown in Figure 1. Each inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Figure 1.
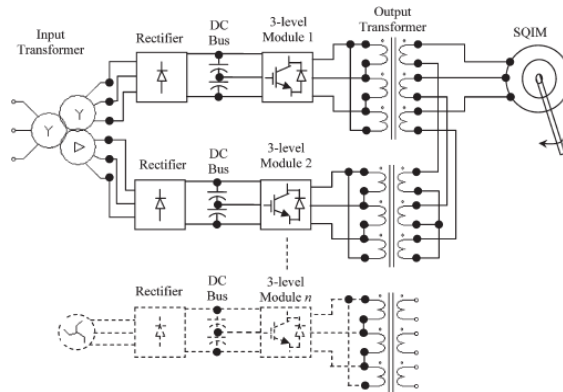
Figure 1: Block Diagram of Three-Phase Three-Level Inverter Modules Connected in Series Driving an SQIM

If "*Vdc*" is the dc-bus voltage of each inverter module, then "*α*" is the turns ratio of each transformer and "*n*" is the number of inverter modules then for sine PWM (SPWM) strategy; the motor rms phase voltage (VPh_motor) can be expressed as follows:

$$\text{rms of } V_{\text{Ph\_motor}} = \sqrt{3}\alpha m n \frac{V_{\text{dc}}}{2\sqrt{2}}$$

(1)

where *m* is the modulation index of the inverter topology defined as follows:

$$m = \frac{\text{peak of } V_{\text{ph\_inverter}}}{n \frac{V_{\text{dc}}}{2}}.$$

(2)

Vph_inverter is the total phase voltage reference of the inverter topology. For the given peak of VPh_motor, peak of Vph_inverter can be computed as follows:

$$\text{peak of } V_{\text{ph\_inverter}} = \frac{\text{peak of } V_{\text{ph\_motor}}}{\sqrt{3}\alpha}.$$

(3)

The generation of individual reference voltage signal of each inverter is discussed as follows. The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, "*n*" numbers of such three-level inverter modules require "2*n*" number of carriers [4], [7]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for *R* phase is shown in Figure 2 for four series-connected three-level inverters. The carrier waves 1 and 1_ (Figure 2) with *R*-phase voltage reference controls the inverter module 1. Similarly, 2–2′, 3–3′, and 4–4′ carrier waves with *R*-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals.
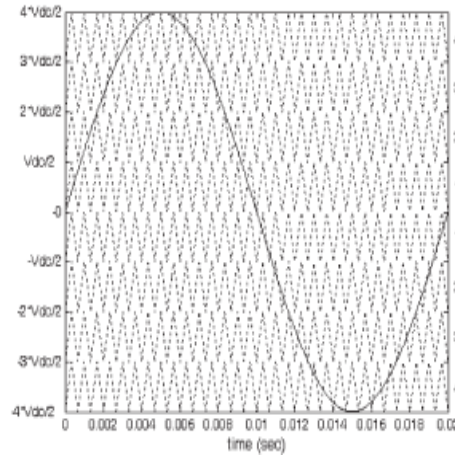
Figure 2: Carrier Waves and the Sinusoidal Modulating VOLTAGE signal for

R phase in SPWM technique

It is important to note that no two three-level inverter modules switch simultaneously (Figure 2). Thus, the maximum *dv/dt* rate of the output voltage of this topology is limited to that of a single three-level inverter module. The references of each inverter are shown in Figure 3. The four windings, one from each transformer, are connected in series and produced the net *R*-phase voltage, as shown in. Similarly, the other two phase voltages are generated.

DESIGN OF INVERTER MODULES

The general configuration of a sensor less SQIM drive with "*n*" number of three-phase voltage source modules connected in series is shown in Figure 1. Each voltage source module consists of a three-phase diode rectifier, a dc bus, a three phase three-level NPC inverter, and a three-phase transformer. In this section, design guidelines are presented for each module to drive a motor of voltage and current ratings *Vs* and *Is*, respectively.

Design of Transformer and Inverter for Each Module

The primary side of each three-phase transformer is chosen as delta connected while the secondary side is kept open for the series connection between the modules. Normally, the dc-bus voltage (Vdc) of each module is chosen such that the standard insulated-gate bipolar transistor (IGBT) module (for example, 1400-V IGBT, 300 A) can be used. Similarly, the current rating (Iinv) of each inverter module is chosen. Now, the current required on the motor side of the transformer is Is. Then, the current drawn from the inverter is Is $\alpha \sqrt{3}$ and must be equal to Iinv. In this paper, α is the transformer turns ratio defined as follows:

$$\alpha = \frac{\text{number of transformer phase turns on the motor side}}{\text{number of transformer phase turns on the inverter side}}$$

(4)

Thus, the turns ratio of the transformer (α) is obtained as follows:

$$\alpha = \frac{I_{inv}}{\sqrt{3} * I_s}.$$

(5)

For n number of modules, the maximum line voltage, which this topology can produce, is $\sqrt{3}\ V$dc$(\alpha\ n/\sqrt{2})$, assuming space-vector PWM (SVPWM) strategy. This voltage must match the required motor line voltage Vs. Thus, the number of modules n can be selected as follows:

$$n = \frac{\sqrt{2} * V_s}{\sqrt{3} * \alpha * V_{dc}} = \frac{\sqrt{2} * V_s * I_s}{V_{dc} * I_{inv}}.$$

(6)

At maximum modulation index in the linear modulation zone, all the modules share the net fundamental output voltages almost equally. In addition, all the modules also have some amount of fifth-, seventh-, and higher order voltage harmonics besides the very small amount of switching harmonics. These voltage harmonics must be taken care of while designing the standard transformer for each module. However, all the module currents, and hence the transformer currents, remain almost sinusoidal.

Selection of DC-Bus Capacitor for Each Module

In single-phase inverters, the dc bus carries second-harmonic currents in addition to the switching currents. Therefore, the size of the capacitors increases when single-phase inverters are used in cascaded H-bridge topology [8]. Since the proposed drive has three-phase inverter at the output stage, the low frequency (second harmonic) ripple in the capacitor will not be present.

Therefore, the size of the capacitor will be relatively small in the case of the proposed topology. If any module fails, the inverter output of the faulty module can be bypassed (by a switch), and the topology can operate with reduced output voltage and hence reduced power. Therefore, for one module failure among "n" number of series connected module, the output voltage will decrease to "$n-1/n$" times although the same output current can be delivered. Hence, the power rating of the drive will decrease to "$n - 1/n$" times.
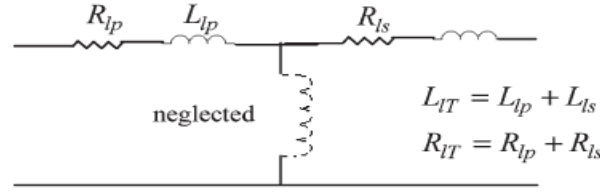
Figure 3: Equivalent Circuit of a Single-Phase Transformer with 1:1 Turns Ratio

SQIM DRIVE USING PROPOSED CONVERTER

The general configuration of a sensor less SQIM drive with "n" number of NPC three-level inverter is shown in Figure 1. All three-level inverters, connected in series, drive the motor and share the load.

Rotor-Flux-Oriented SQIM

In this topology, the stator leakage inductance value has to be modified to incorporate the leakage inductance of the output transformers (LlT). In addition, the effective stator resistance changes due to the presence of transformer winding resistances (RlT). By neglecting the magnetizing branch of the inverter transformer, the equivalent circuit of the transformer is a simple R–L circuit, as shown in Figure 3. Thus, the modified values of the stator leakages are as follows:

$$\sigma L_s' = \sigma L_s + L_{lT}$$
$$R_s' = R_s + R_{lT}.$$

(7)

Hence, the modified dynamical equations of the SQIM voltages and currents in the d–q plane are presented as follows:

$$V_{sd} = R_s' i_{sd} + \sigma L_s' \frac{di_{sd}}{dt} - \underline{\sigma L_s' \omega_{mr} i_{sq}} + \frac{1}{(1+\sigma_r)} \frac{d\psi_r}{dt}$$

(8)

$$V_{sq} = R_s' i_{sq} + \sigma L_s' \frac{di_{sq}}{dt} + \underline{\sigma L_s' \omega_{mr} i_{sd}} + \frac{\psi_r \omega_{mr}}{(1+\sigma_r)}$$

(9)

where the d-axis is aligned with the rotor flux vector (ψr)[17], [21]. The rotor flux vector in stationary coordinates (_ψrs) is expressed in terms of stator flux as

$$\vec{\psi}_{rs} = \frac{L_r}{L_0} \{\vec{\psi}_s - \sigma L_s \vec{i}_s\}.$$

(10)

The stator flux ψs is estimated from the stator voltage _Vs as follows:

$$\vec{\psi}_s = \int (\vec{V}_s - R_s \vec{i}_s - \omega_c \vec{\psi}_s).$$

(11)

The problem integration at low frequency is tackled by replacing the pure integration of stator voltage with a low-pass filter (cutoff frequency = ωc) [9], [11].

Motor Controller

The d- and the q-axis motor-voltage equations (9) and (10) show the first-order dynamics of the stator currents (isd and isq) if the underlined terms are decoupled. Therefore, simple PI controllers with unity feedback system can control

the d–q-axis motor currents to control the flux and the torque of the motor, as shown in Figure 4.
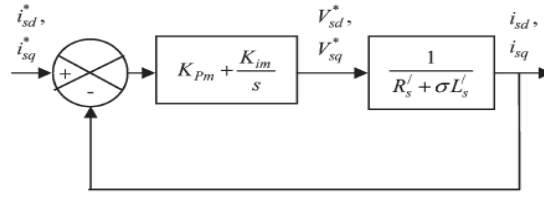

Figure 4: d- and q-Axis Motor Current Controller

By choosing the proper gain values of the PI controllers, the desired bandwidth ($1/\tau im$) of the motor current controller is achieved [11]. Thus, the closed loop transfer functions of *isd* and *isq* become as follows:

$$\frac{i_{sd}(s)}{i_{sd}^*(s)} = \frac{1}{1 + s\tau_{im}}$$
$$\frac{i_{sq}(s)}{i_{sq}^*(s)} = \frac{1}{1 + s\tau_{im}}.$$

(12)

In this paper, the desired response time *τim* of the motor current is chosen as 4 ms. Finally, the outputs of the PI controllers are added to the underlined coupling terms of (9) and (10) to get the actual *d*- and *q*-axis voltage references ($V\,^*_{sd}$, $V\,^*_{sq}$) [17]. It is important to note that the motor phase voltages and the inverter phase voltages are not in phase. The motor phase voltage is in phase with the line voltages of the inverter modules. Hence, a phase shift of 30∘ is provided to the three motor phase voltage references obtained to generate the three inverter phase voltage references. The phase reference obtained is the total phase reference of the topology. Hence, this reference is obtained by adding the reference of the individual inverter modules. The input transformer with a delta and wye secondary for two three-level modules is shown in Figure 1. If more number of modules is used, then the same secondary delta and wye can be loaded with parallel connections as an isolated dc bus is not required. This is in contrast to the cascaded H-bridge topology, which requires an isolated dc bus for each module. However, if the input current needs to be shaped, the input transformer with zigzag secondary can be used.

BLDC Motor

The BLDC motor is an AC synchronous motor with permanent magnets on the rotor (moving part) and windings on the stator (fix part). Permanent magnets create the rotor flux. The energized stator windings create electromagnet poles. The rotor (equivalent to a bar magnet) is attracted by the energized stator phase, generating a rotation. By using the appropriate sequence to supply the stator phases, a rotating field on the stator is created and maintained. This action of the rotor - chasing after the electromagnet poles on the stator - is the fundamental action used in synchronous permanent magnet motors. The lead between the rotor and the rotating field must be controlled to produce torque. This synchronization implies knowledge of the rotor position.
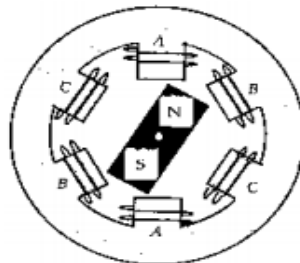
Figure 5: A 3-Phase Synchronous Motor with a Single Permanent Magnet Pair Pole Rotor

On the stator side, three phase motors are the most common. These offer a good compromise between precise control and the number of power electronic devices required to control the stator currents. For the rotor, a greater number of poles usually create a greater torque for the same level of current. On the other hand, by adding more magnets, a point is reached where, because of the space needed between magnets, the torque no longer increases. The manufacturing cost also increases with the number of poles. As a consequence, the number of poles is a compromise between cost, torque and volume.

The BLDC Motor Control:

The key to effective torque and speed control of a BLDC motor is based on relatively simple torque and Back EMF equations, which are similar to those of the DC motor. The Back EMF magnitude can be written as:

$$E = 2NlrB\omega$$

(13)

And the torque term as

$$T = \left(\frac{1}{2}i^2 \frac{dL}{d\theta} \right) - \left(\frac{1}{2}B^2 \frac{dR}{d\theta} \right) + \left(\frac{4N}{\pi}Brl\pi i \right)$$

(14)

Where N is the number of winding turns per phase, l is the length of the rotor, r is the internal radius of the rotor, B is the rotor magnet flux density, ω is the motor's angular velocity, i is the phase current, L is the phase inductance, θ is the rotor position, R is the phase resistance.

## MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in different cases, in that 1). Implementation of Series-Connected Three-Level Inverter Topology Applied to Squirrel Cage Induction Machine Drive. 2). Implementation of Series-Connected Multilevel Inverter Topology Applied to BLDC Machine Drive.

Case 1: Implementation of Series-Connected Three-Level Inverter Topology Applied to Squirrel Cage Induction Machine Drive
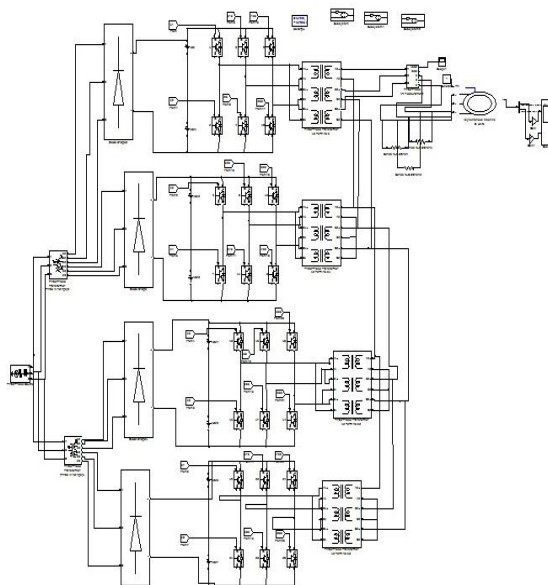

**Figure 6: Matlab/Simulink Model of Proposed Series-Connected Three-Level Inverter
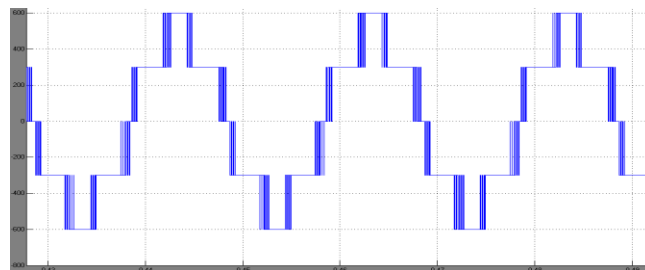Topology Applied to Squirrel Cage Induction Machine Drive**

Figure 6 shows the block diagram of proposed series connected multilevel inverter fed induction motor drive. It consists of four inverters. Here we are using phase shifted carrier PWM.
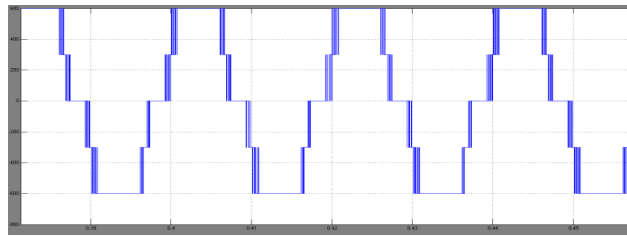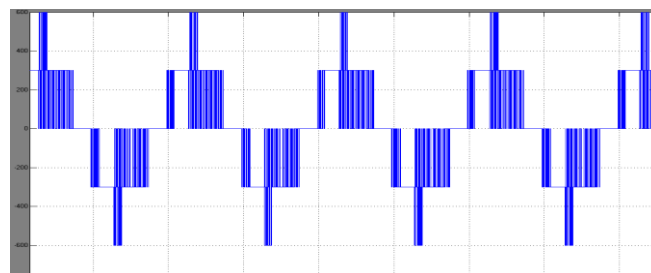

Figure 7: Three Level Output Inverter 1
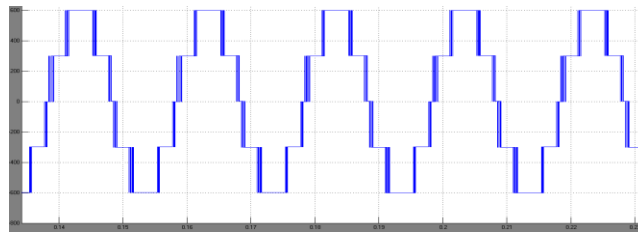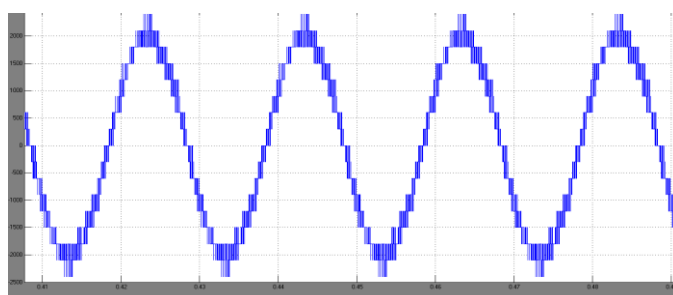

Figure 8: Three Level Output Inverter2

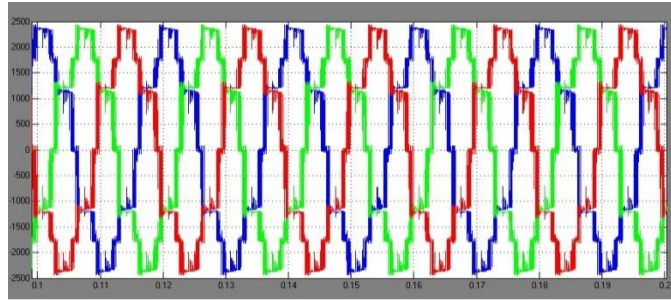**Figure 9: Three Level Output Inverter3**

Figure 10: Three Level Output Inverter4

Figure 7 to 10 shows the individual inverter outputs. From the figures it is clear that each output consists of only three levels.
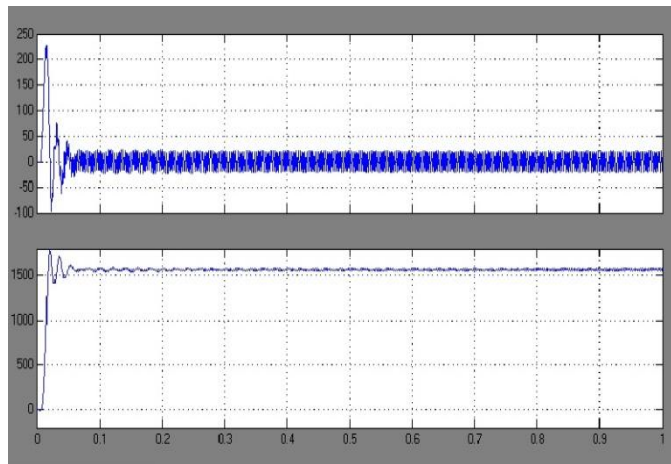

Figure 11: Multilevel Output

Figure 12: Multilevel Output Three Phase

Figure 12 shows the waveform represents the output voltage of the three phase multilevel inverter.

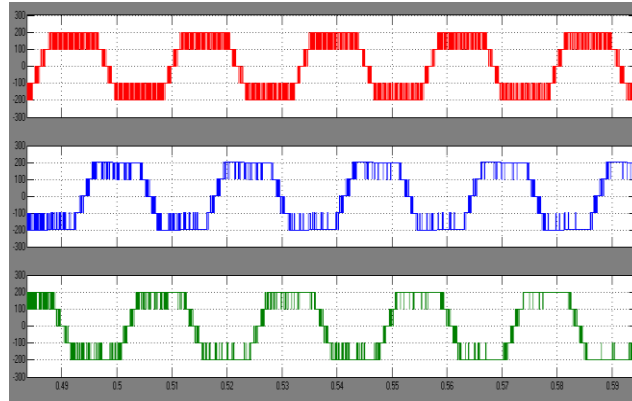**Figure 13: Electromagnetic Torque and Speed Curves of SQCIM**

Figure 13 represents the Electromagnetic Torque and rotor speed characteristics of the Squirrel cage Induction motor.

Case 2: Implementation of Series-Connected Multilevel Inverter Topology Applied to BLDC Machine Drive.
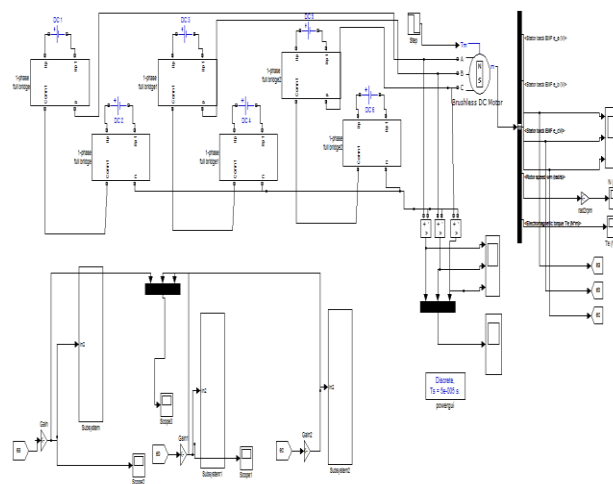

**Figure 14: Matlab/Simulink Model of Proposed Series-Connected Multilevel
Inverter Topology Applied to BLDC Machine Drive**

Figure 14 shows the block diagram of proposed series connected multilevel inverter fed BLDC drive.

Figure 15: Output Voltage of Proposed Series Connected Multilevel Inverter fed BLDC Drive

Figure 15 shows the Output Voltage of proposed series connected multilevel inverter fed BLDC drive.
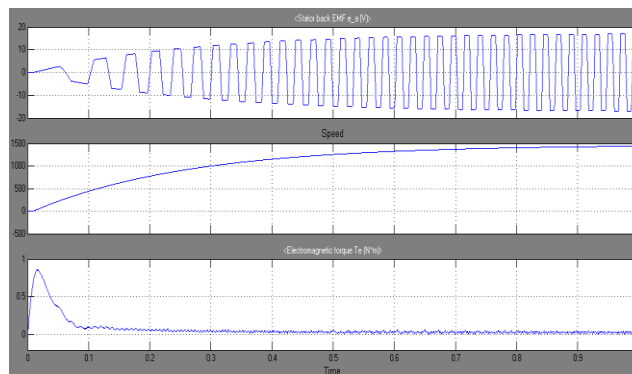
Figure 16: Back EMF, Speed, Electromagnetic Torque

Figure 16 shows the Back EMF, Speed, Electromagnetic Torque of proposed series connected multilevel inverter fed BLDC drive.

CONCLUSIONS

A series connection of three-level inverters has been proposed for a medium-voltage SQIM drive and multilevel inverter with BLDC machine drive also proposed, with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc bus capacitor and reduced imbalance problems in the dc bus are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses that's why here we implement the proposed system in multilevel topology we get better response as well as many advantages compared to three level inverter. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies. In this paper conventional and the cascaded multilevel inverter topologies were discussed and results were placed. Finally a Matlab/Simulink model is developed and simulation results are presented.

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AUTHORS DETAILS

CH.BRAHMAIAH received his B.tech degree from Prakasam Engineering college in the year 2011 and he pursuing his masters in power electronics & Electrical drives from C.V.S.R college of engineering (Autonomous),

Hyderabad, His areas of Interests include power electronics, electrical machines & industrial drives.

CH.SRINIVAS RAO did AMIE from Institute of engineers, Kolkata M.E from Osmania university. Industrial experience about 20 years and teaching experience 5 years. Presently he is a Associate professor of EEE department, in C.V.S.R Engineering college.

M. BABA FAKRUDDIN received his B.Tech degree from G.PullaReddy College of Engineering and Technology (Autonomous) in the year 2009, and he is pursuing his Masters in Power Electronics & Electrical drives from C.V.S.R college of engineering (Autonomous), Hyderabad. His areas of interests include Power Electronics, Electrical Machines& Power Drives